An orthogonal 6F/sup 2/ trench-sidewall vertical device cell for 4 Gb/16 Gb DRAM

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This paper appears in: **Electron Devices Meeting, 2000. IEDM Technical Digest. International**
On page(s): 349 - 352
10-13 Dec. 2000
San Francisco, CA, USA
2000
ISBN: 0-7803-6438-4
IEEE Catalog Number: 00CH37138
Number of Pages: 871
References Cited: 8
INSPEC Accession Number: 6880860

Abstract:
This paper describes a novel 6F/sup 2/ trench-capacitor DRAM with a trench-sidewall vertical-channel array transistor. The cell features a line/space pattern for the active area, single-sided buried-strap node contact, vertical transistor channel formed along the upper region of the trench capacitor, a device active area bounded by the isolation trench and capacitor collar, and a single bit contact per cell.

Index Terms:
isolation technology cellular arrays DRAM chips MOS memory circuits trench-sidewall vertical device cell trench-capacitor DRAM line/space pattern single-sided buried-strap node contact device active area isolation trench capacitor collar single bit contact 4 Gbit 16 Gbit

A 0.135 /spl mu/m/sup 2/ 6F/sup 2/ trench-sidewall vertical device cell for 4 Gb/16 Gb DRAM

- Radens, C.J. Gruening, U. Mandelman, J.A. Seitz, M. Lea, D. Casarotto, D. Clevenger, L. Nesbit, L. Malik, R. Halle, S. Kudelka, S. Tews, H. Divakaruni, R. Sim, J. Strong, A. Tibbel, D. Arnold, N. Bukofsky, S. Preuninger, J. Kunkel, G. Bronner, G.
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This paper appears in: **VLSI Technology, 2000. Digest of Technical Papers. 2000 Symposium on**
On page(s): 80 - 81
13-15 June 2000
Honolulu, HI, USA
2000
ISBN: 0-7803-6305-1
IEEE Catalog Number: 00CH37104
Number of Pages: xv+226
References Cited: 7
INSPEC Accession Number: 6671145

Abstract:
A 0.135 /spl mu/m/sup 2/ trench-capacitor DRAM cell with a trench-sidewall vertical-channel array device has been fabricated using 150 nm groundrules and optical lithography. This 6F/sup 2/ cell features a novel active area layout, a trench-top-oxide (TTO) isolation between trench capacitor and trench gate, maskless self-aligned buried strap node contact, shallow trench isolation (STI), a self-aligned poly-plug bit contact, and two levels of bitline interconnect, both formed using a W dual-damascene process.

Index Terms:
DRAM chips isolation technology integrated circuit metallisation 6F/sup 2/ trench-sidewall vertical-channel array device trench-capacitor DRAM cell optical lithography trench-top-oxide isolation maskless self-aligned buried strap node contact shallow trench isolation self-aligned poly-plug bit contact bitline interconnect W dual-damascene process 4 Gbit 16 Gbit 150 nm W

A highly cost efficient 8F/sup 2/ DRAM cell with a double gate vertical transistor device for 100 nm and beyond

- Weis, R. Hummler, K. Akatsu, H. Kudelka, S. Dyer, T. Seitz, M. Scholz, A. Kim, B. Wise, M. Malik, R. Strane, J. Goebel, Th. McStay, K. Beintner, J. Arnold, N. Gerber, R. Liegl, B. Knorr, A. Economikos, L. Simpson, A. Yan, W. Dobuzinsky, D. Mandelman, J. Nesbit, L. Radens, C.J. Divakaruni, R. Bergner, W. Bronner, G. Mueller, W.
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This paper appears in: **Electron Devices Meeting, 2001. IEDM Technical Digest. International**
On page(s): 18.7.1 - 18.7.4
2-5 Dec. 2001
Washington, DC, USA
2001
ISBN: 0-7803-7050-3
IEEE Catalog Number: 01CH37224
Number of Pages: 951
References Cited: 5
INSPEC Accession Number: 7238988

Abstract:
This paper describes a highly cost efficient 8F/sup 2/ trench capacitor DRAM cell with a lithography-friendly layout. It consists of only 4 critical masks, i.e. a highly regular trench pattern and three line masks. The cell is shrinkable below 100 nm. It is fabricated with an overlay robust process with a double gate vertical pass transistor in the upper part of the trench capacitor and a double buried strap node contact. The cell features four bitline contacts per cell (two shared with the neighboring cells). Lines of deep oxide isolation trenches provide efficient decoupling of adjacent cells. Feasibility has been demonstrated at a 175 nm design rule with a 128 Mb product chip and a 1 Mb test array at 120 nm.

Index Terms:
DRAM chips masks integrated circuit layout isolation technology cost efficient 8F/sup 2/ trench capacitor DRAM cell double gate vertical transistor lithography-friendly layout critical masks regular trench pattern line masks shrinkable cell overlay robust process double buried strap node contact bitline contacts deep oxide isolation trenches adjacent cell decoupling 100 nm 175 nm 128 Mbit 120 nm

Array transistor design challenges in trench capacitor DRAM technology

- Yujun Li Jai-Hoon Sim Mandelman, J. McStay, K. Qiuyi Ye Bronner, G.

This paper appears in: **VLSI Technology, Systems, and Applications, 2001. Proceedings of Technical Papers. 2001 International Symposium on**
On page(s): 85 - 88
18-20 April 2001
Hsinchu, Taiwan
2001
ISBN: 0-7803-6412-0
IEEE Catalog Number: 01TH8517
Number of Pages: 310
References Cited: 7
INSPEC Accession Number: 7068833

Abstract:
BuriEd Strap Trench (BEST) array cell design has been extended for more than 4 generations. However, significant scaling challenges in planar trench DRAM technology will be encountered below the 0.1 /spl mu/m generation. In this paper, we review the key factors that limit the scaling of the BEST array cell, further analyze the scaling challenges considering design for manufacturability, and finally discuss other design and/or technology innovations including the vertical array transistor to overcome scaling limitations.

Index Terms:
DRAM chips capacitors design for manufacture planar trench capacitor DRAM technology buried strap trench array cell device scaling BEST array cell design for manufacturability vertical array transistor 0.1 micron

A novel trench DRAM cell with a vertical access transistor and buried strap (VERI BEST) for 4 Gb/16 Gb

- Gruening, U. Radens, C.J. Mandelman, J.A. Michaelis, A. Seitz, M. Arnold, N. Lea, D. Casarotto, D. Knorr, A. Halle, S. Ivers, T.H. Economikos, L. Kudelka, S. Rahn, S. Tews, H. Lee, H. Divakaruni, R. Welser, J.J. Furukawa, T. Kanarsky, T.S. Alsmeier, J. Bronner, G.B.
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This paper appears in: **Electron Devices Meeting, 1999. IEDM Technical Digest. International**
On page(s): 25 - 28
5-8 Dec. 1999
Washington, DC, USA
1999
ISBN: 0-7803-5410-9
IEEE Catalog Number: 99CH36318
Number of Pages: 943
References Cited: 5
INSPEC Accession Number: 6506880

Abstract:
Results are presented for a novel trench capacitor DRAM cell using a vertical access transistor along the storage trench sidewall which effectively decouples the gate length from the lithographic groundrule. A unique feature of this cell is the vertical access transistor in the array which is self-aligned to the buried strap connection of the storage trench (VERI BEST) and bounded by trench isolation oxide. The VERI BEST cell concept, process and electrical results obtained from 8F/sup 2/ test cell arrays at 0.175 /spl mu/m groundrules are described in this paper.

Index Terms:
DRAM chips DRAM cell vertical access transistor buried strap VERI BEST trench capacitor storage trench sidewall self-aligned array trench isolation oxide 0.175 micron 4 Gbit 16 Gbit